What is claimed is:

1. A semiconductor device having a mode of functional test comprising:

a circuit block to which an input signal is input at an input clock and which outputs an output signal of the value corresponding to said input signal;

a first signal path for guiding a test input signal, which has been supplied to a first pad, to the signal input terminal of said circuit block;

a second signal path for guiding a test clock which has been supplied to a second pad, to the clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from the signal output terminal of said circuit block, to a third pad; and

a delay measuring signal path for measuring the wiring delay time of said first, second, or third signal path.

2. The semiconductor device having a mode of functional test, according to Claim 1, wherein said first signal path comprises a selector which, during a normal operation, supplies an output signal from the preceding circuit block to said signal input terminal of said circuit block and, during a test operation, supplies said test input signal to said signal input terminal of said circuit block.

3. The semiconductor device having a mode of functional test, according to Claim 1, wherein said second signal path comprises a selector which, during a normal operation, supplies

the normal clock to said signal input terminal of said circuit block and, during a test operation, supplies said test clock to said signal input terminal of said circuit block.

4. The semiconductor device having a mode of functional test, according to Claim 1, wherein said third signal path comprises a selector which, during a normal operation, supplies a prescribed signal other than said test output signal to said third pad during a normal operation and, during a test operation, supplies said test output signal to said third pad during a test operation.

5. The semiconductor device having a mode of functional test, according to Claim 1, wherein said delay measuring signal path comprises a signal path for guiding said test clock input to said clock input terminal to a fourth pad.

6. The semiconductor device having a mode of functional test, according to Claim 5, wherein said third signal path and said delay measurement signal path are formed so that the wiring delay time of said third signal path and the wiring delay time of said measurement signal path are substantially the same.

7. The semiconductor device having a mode of functional test, according to Claim 5, wherein said delay measurement signal path comprises a selector which, during a normal operation, supplies a prescribed signal other than said test clock to said fourth pad and, during a test operation, supplies said test clock to said fourth pad.

8. The semiconductor device having a mode of functional test, according to Claim 1, comprising a selector which supplies

said test output signal input through said third signal path or said test clock input through said delay measurement signal path to said third pad during a test operation.

9. The semiconductor device having a mode of functional test, according to Claim 8, wherein said selector selects said test output signal or said test clock according to the value of the mode signal input from outside during a test operation.

10. The semiconductor device having a mode of functional test, according to Claim 8, wherein said third signal path and said delay measurement signal path are formed so that the wiring delay time of said third signal path and the wiring delay time of said delay measurement signal path are substantially the same.

11. The semiconductor device having a mode of functional test, according to Claim 8, wherein said selector selects a prescribed signal other than said test output signal and said test clock and supplies that signal to said third pad during a normal operation.

12. The semiconductor device having a mode of functional test, according to Claim 1, wherein said third signal path comprises a dummy latch for introducing said test output signal and a signal path for guiding the output of the latch to said third pad; and said delay measurement signal path comprises a signal path for guiding said test output signal to a fourth pad.

13. The semiconductor device having a mode of functional test, according to Claim 12, wherein said dummy latch is constituted so as to introduce said test output signal at substantially the same operating speed as the latch for

introducing the output signal of said circuit block during a normal operation.

14. The semiconductor device having a mode of functional test, according to Claim 12, wherein said third signal path is formed so that the wiring delay time from said signal output terminal of said circuit block to said dummy latch is substantially the same as the wiring delay time from said signal output terminal of said circuit block to said latch.

15. The semiconductor device having a mode of functional test, according to Claim 12, wherein the delay measurement signal path comprises a selector which, during a normal operation, supplies a prescribed signal other than said test output signal to said fourth pad and, during a test operation, supplies said test output signal to said fourth pad.

16. The semiconductor device having a mode of functional test, according to Claim 1, wherein said delay measurement signal path comprises a selector which supplies said test input signal or said test clock to fourth pad during a test operation.

17. The semiconductor device having a mode of functional test, according to Claim 16, wherein said selector selects said test input signal or said test clock according to the value of the mode signal input from outside during a test operation.

18. The semiconductor device having a mode of functional test, according to Claim 16, wherein the delay measurement signal path is formed so that the wiring delay time when said test input signal is input to said selector is substantially the same as the wiring delay time when said test clock is input to said

selector.

19. The semiconductor device having a mode of functional test, according to Claim 16, wherein said selector supplies a prescribed signal other than said test input signal and said test clock to said fourth pad during a normal operation.

20. The semiconductor device having a mode of functional test, according to Claim 1, wherein said circuit block is a macro cell.